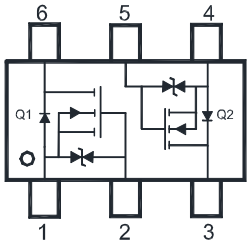
MMBT7002KD-AH

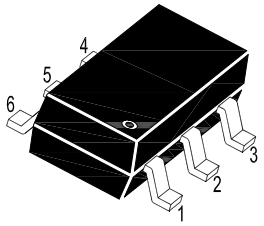
Dual N-Channel Enhancement Mode MOSFET

Features

- AEC-Q101 Qualified
- Low on resistance $R_{DS(ON)}$
- Low gate threshold voltage
- Low input capacitance
- Halogen and Antimony Free(HAF), RoHS compliant
- Typical ESD Protection HBM Class 2

Classification	Voltage Range(V)
0A	< 125
0B	125 to < 250
1A	250 to < 500
1B	500 to < 1000
1C	1000 to < 2000
2	2000 to < 4000
3A	4000 to < 8000
3B	≥ 8000





1.Source 2. Gate 3. Drain
4. Source 5.Gate 6. Drain
SOT-26 Plastic Package

Application

- Portable appliances
- Battery management

Absolute Maximum Ratings (T_a = 25℃) (Q1\Q2)

Parameter	Symbol	Value	Unit
Drain Source Voltage	V_{DS}	60	V
Gate Source Voltage	V_{GS}	± 20	V
Drain Current	I_D	300	mA
Peak Drain Current, Pulsed [1)]	I_{DM}	1	A
Power Dissipation	P_{tot}	350	mW
Operating and Storage Temperature Range	T_j, T_{stg}	- 55 to + 150	℃

Thermal Resistance Ratings

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Ambient [2)]	$R_{\theta JA}$	357	℃/W

[1)] Pulse Test: Pulse Width ≤ 100 μs, Duty Cycle ≤ 2%,Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$.

[2)] Device mounted on FR-4 substrate PC board, with minimum recommended pad layout.

Dated: 26/03/2021 IMC1 Rev:01

Characteristics at T_a = 25℃ unless otherwise specified(Q1\Q2)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Drain Source Breakdown Voltage at I_D = 10 µA	$V_{(BR)DSS}$	60	-	-	V
Zero Gate Voltage Drain Current at V_{DS} = 60 V	I_{DSS}	-	-	1	µA
Gate Source Leakage Current at V_{GS} = ± 20 V	I_{GSS}	-	-	± 10	µA
Gate Source Threshold Voltage at V_{DS} = V_{GS}, I_D = 250 µA	$V_{GS(th)}$	1	-	2.5	V
Static Drain Source On-State Resistance at V_{GS} = 10 V, I_D = 500 mA at V_{GS} = 4.5 V, I_D = 200 mA	$R_{DS(on)}$	- -	- -	3 4	Ω
DYNAMIC PARAMETERS					
Forward Transconductance at V_{DS} = 10 V, I_D = 200 mA	g_{FS}	80	-	-	mS
Gate Resistance at V_{GS} = 0 V, V_{DS} = 0 V, f = 1MHz	R_g	-	200	-	Ω
Input Capacitance at V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	21	-	pF
Output Capacitance at V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	-	12	-	pF
Reverse Transfer Capacitance at V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	-	0.35	-	pF
Gate charge total at V_{DS} =10 V, I_D = 0.5 A, V_{GS} = 4.5 V	Q_g	-	0.4	-	nC
Gate to Source Charge at V_{DS} =10 V, I_D = 0.5 A, V_{GS} = 4.5 V	Q_{gs}	-	0.2	-	nC
Gate to Drain Charge at V_{DS} =10 V, I_D = 0.5 A, V_{GS} = 4.5 V	Q_{gd}	-	0.1	-	nC
Turn-On Delay Time at V_{DS} = 30 V, V_{GS} = 10 V, I_D = 0.5 A, R_G = 25 Ω	$t_{d(on)}$	-	2.7	-	ns
Turn-On Rise Time at V_{DS} = 30 V, V_{GS} = 10 V, I_D = 0.5 A, R_G = 25 Ω	t_r	-	2.5	-	ns
Turn-Off Delay Time at V_{DS} = 30 V, V_{GS} = 10 V, I_D = 0.5 A, R_G = 25 Ω	$t_{d(off)}$	-	13	-	ns
Turn-Off Fall Time at V_{DS} = 30 V, V_{GS} = 10 V, I_D = 0.5 A, R_G = 25 Ω	t_f	-	8	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at V_{GS} = 0 V, I_S = 0.5 A	V_{SD}	-	0.85	-	V
Body-Diode Continuous Current	I_S	-	-	300	mA
Body Diode Reverse Recovery Time at I_S = 0.5 A, di/dt = 100 A / µs	t_{rr}	-	30	-	ns
Body Diode Reverse Recovery Charge at I_S = 0.5 A, di/dt = 100 A / µs	Q_{rr}	-	29	-	nC

Electrical Characteristics Curves(Q1/Q2)

Fig. 1 Typical Output Characteristic

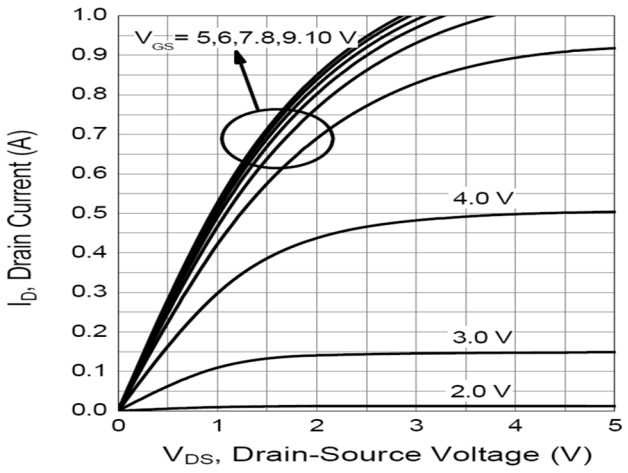


Fig. 2 Gate Threshold Variation vs. T_j

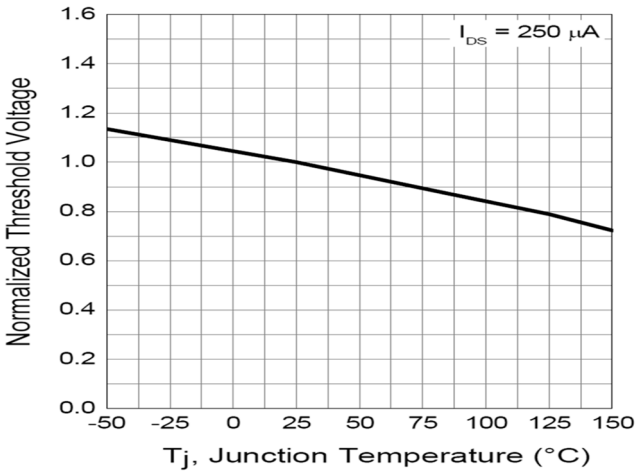


Fig. 3 $R_{DS(on)}$ vs. Gate-Source Voltage

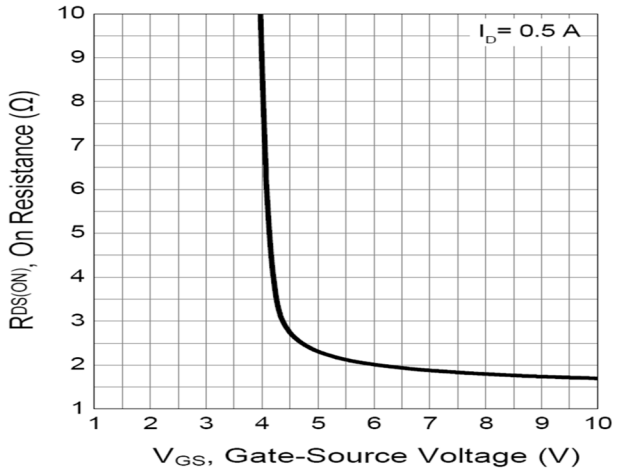


Fig. 4 on-Resistance vs.T_j

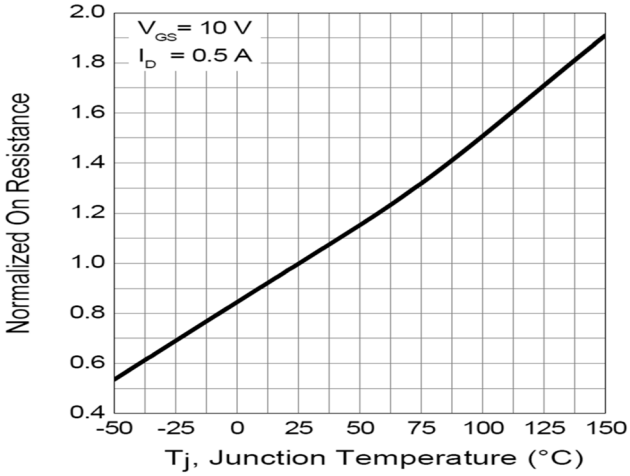


Fig. 5 on-Resistance vs. Drain Current

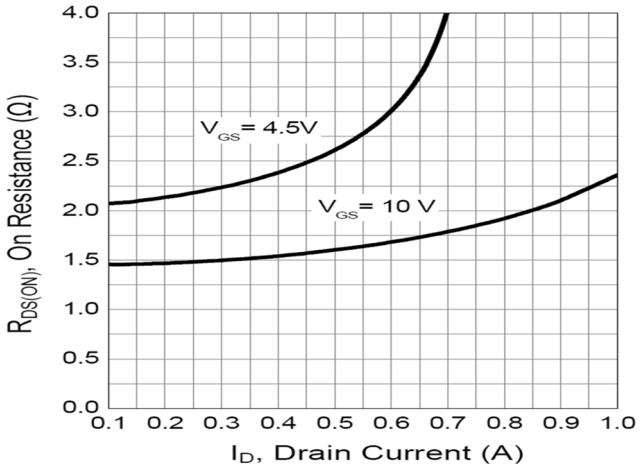
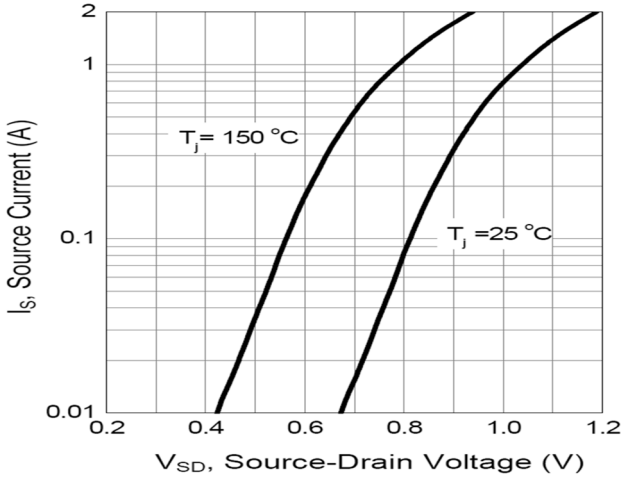


Fig. 6 Typical Forward Characteristic



Electrical Characteristics Curves(Q1\Q2)

Fig. 7 Typical Junction Capacitance

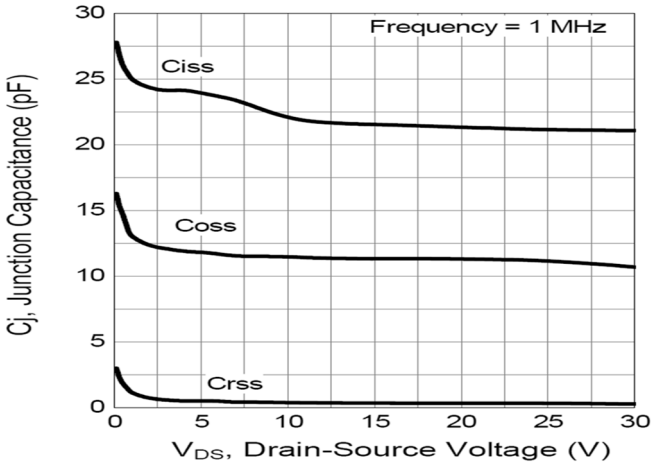
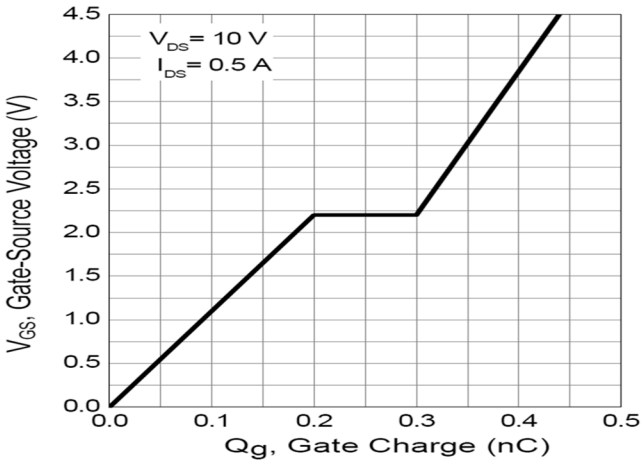


Fig. 8 Gate Charge



Test Circuits

Fig.1-1 Switching times test circuit

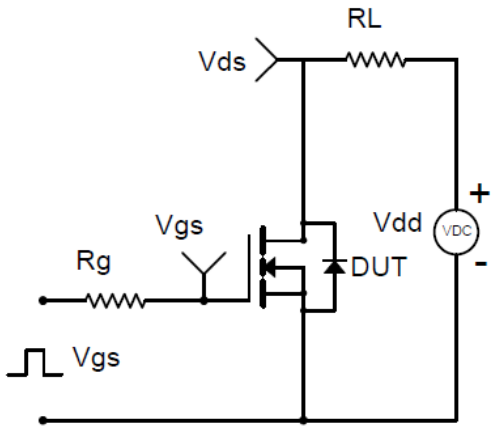


Fig.1-2 Switching Waveform

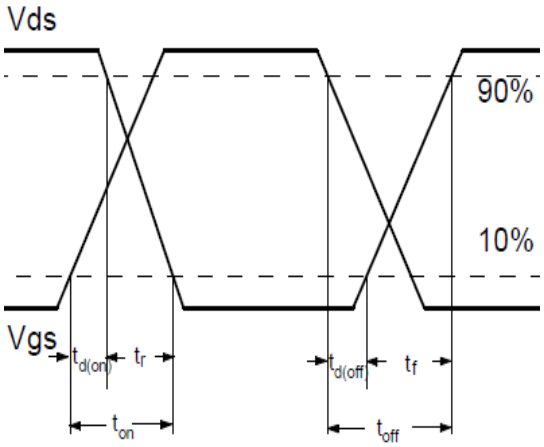


Fig.2-1 Gate charge test circuit

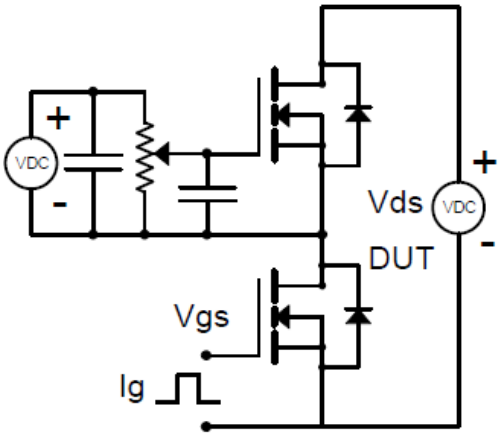
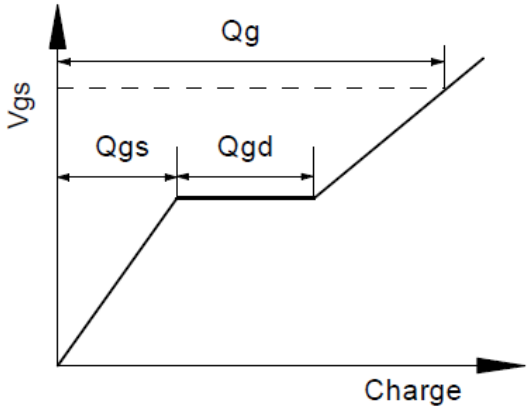
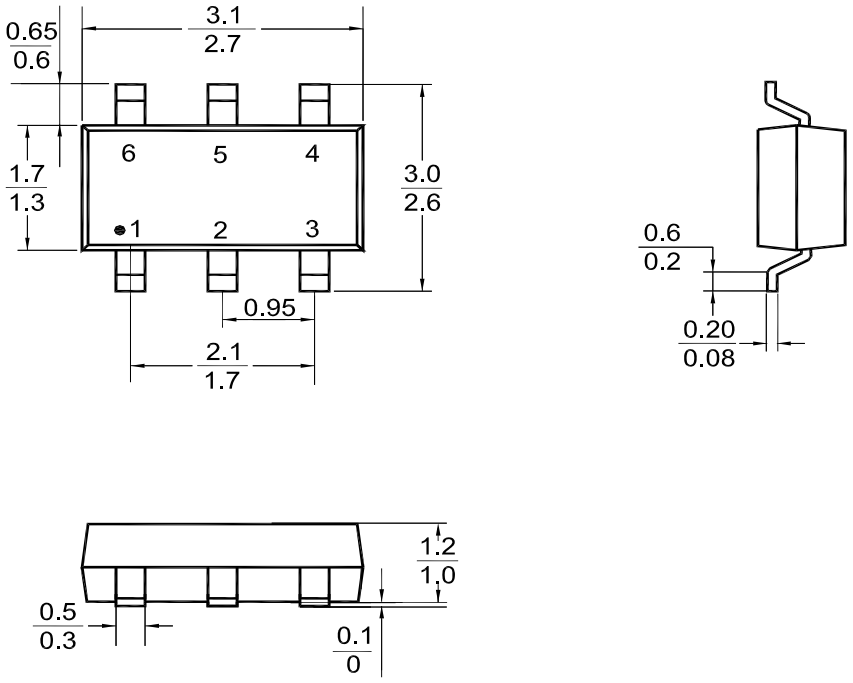


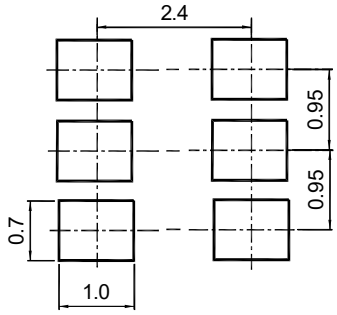
Fig.2-2 Gate charge waveform



Package Outline Dimensions (Units: mm) SOT-26



Recommended Soldering Footprint



Packing information

Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
SOT-26	8	4 ± 0.1	0.157 ± 0.004	178	7	3,000

Marking information

" K712 " = Part No.
" • " = HAF (Halogen and Antimony Free)
"YM" = Date Code Marking
"Y" = Year
"M" = Month
Font type: Arial