

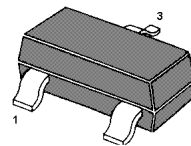
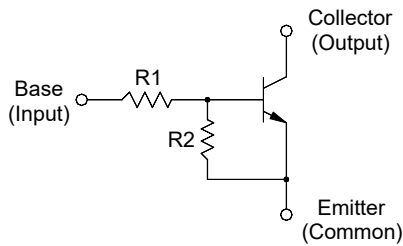
MMBTRC107SS~MMBTRC109SS

NPN Silicon Epitaxial Planar Transistor

for switching and interface circuit and drive circuit applications

Features

- With built-in bias resistors
- Simplify circuit design
- Reduce a quantity of parts and manufacturing process



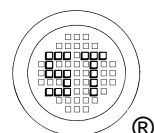
1. Base 2. Emitter 3. Collector
TO-236 Plastic Package

Resistor Values

Type	R1 (KΩ)	R2 (KΩ)
MMBTRC107SS	10	47
MMBTRC108SS	22	47
MMBTRC109SS	47	22

Absolute Maximum Ratings (T_a = 25 °C)

Parameter		Symbol	Value	Unit
Output Voltage		V _o	50	V
Input Voltage	MMBTRC107SS	V _i	30, -6	V
	MMBTRC108SS		40, -7	
	MMBTRC109SS		40, -15	
Output Current		I _o	100	mA
Total Power Dissipation		P _{tot}	200	mW
Junction Temperature		T _j	150	°C
Storage Temperature Range		T _{stg}	- 55 to + 150	°C

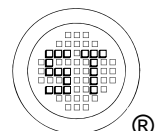


MMBTRC107SS~MMBTRC109SS

Characteristics at $T_a = 25\text{ }^{\circ}\text{C}$

Parameter		Symbol	Min.	Typ.	Max.	Unit
DC Current Gain at $V_O = 5\text{ V}$, $I_O = 10\text{ mA}$	MMBTRC107SS MMBTRC108SS MMBTRC109SS	G_I	80 80 70	- - -	- - -	- - -
Output Cutoff Current at $V_O = 50\text{ V}$		$I_{O(OFF)}$	-	-	500	nA
Input Current at $V_I = 5\text{ V}$	MMBTRC107SS MMBTRC108SS MMBTRC109SS	I_I	- - -	- - -	0.88 0.36 0.16	mA
Output Voltage at $I_O = 10\text{ mA}$, $I_I = 0.5\text{ mA}$		$V_{O(ON)}$	-	-	0.3	V
Input Voltage (ON) at $V_O = 0.2\text{ V}$, $I_O = 5\text{ mA}$	MMBTRC107SS MMBTRC108SS MMBTRC109SS	$V_{I(ON)}$	- - -	- - -	1.8 2.6 5.8	V
Input Voltage (OFF) at $V_O = 5\text{ V}$, $I_O = 0.1\text{ mA}$	MMBTRC107SS MMBTRC108SS MMBTRC109SS	$V_{I(OFF)}$	0.5 0.6 1.5	- - -	- - -	V
Transition Frequency at $V_O = 10\text{ V}$, $I_O = 5\text{ mA}$		$f_T^{1)}$	-	200	-	MHz

¹⁾ Characteristic of transistor only.



MMBTRC107SS~MMBTRC109SS

Electrical Characteristics Curves (MMBTRC108SS)

Fig 1. Output Current Vs. Input Voltage

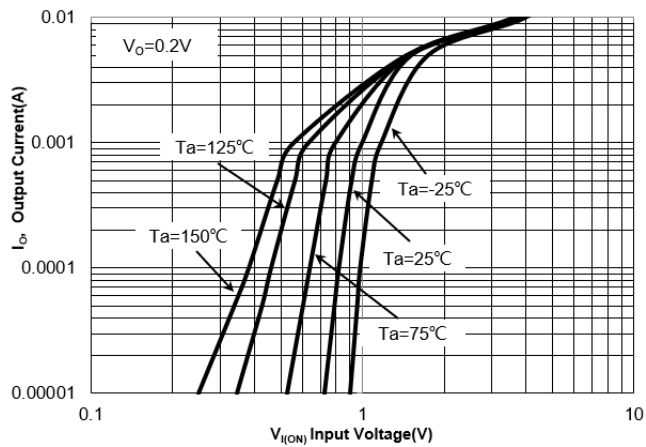


Fig 2. Output Current Vs. Input Voltage

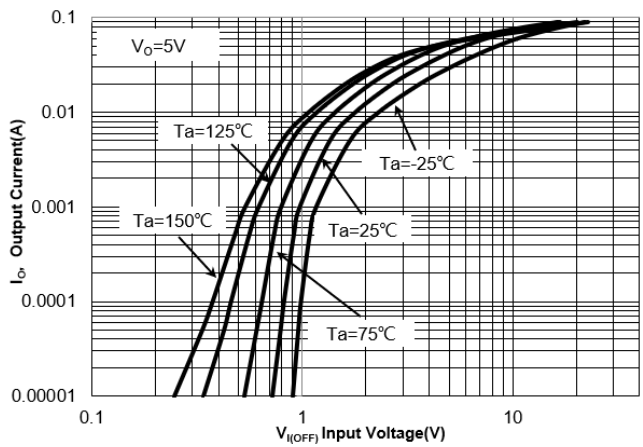


Fig 3. DC Current Gain Vs. Output Current

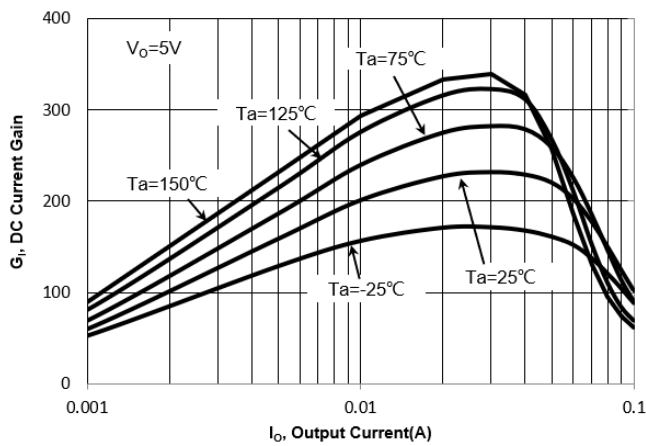


Fig 4. Output Voltage Vs. Output Current

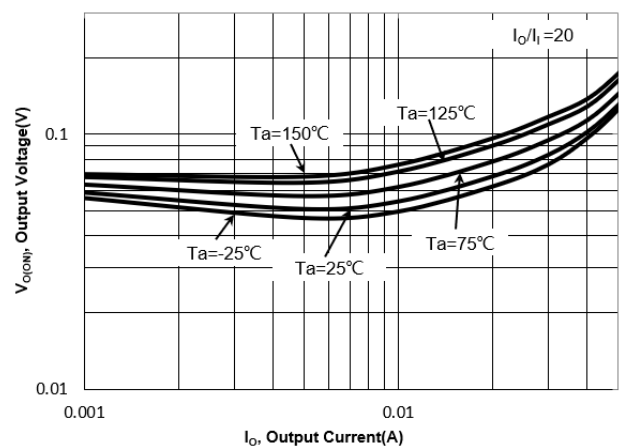


Fig 5. Power Derating Curve

