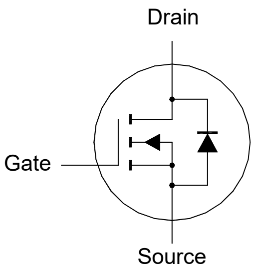
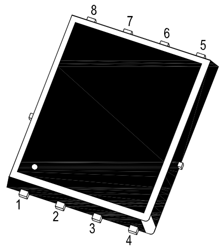
WTM510N062L-HAF

N-Channel Enhancement Mode MOSFET

Features

- Low $R_{DS(ON)}$
- Logic Driven
- Halogen and Antimony Free(HAF), RoHS compliant





1. Source 2. Source 3. Source 4. Gate
5. Drain 6. Drain 7. Drain 8. Drain
DFN5060 Plastic Package

Applications

- Synchronous Rectification for Quick Charger 3.0
- Synchronous Rectification for AC/DC adapter and DC/DC brick power

Absolute Maximum Ratings (T_a = 25℃ unless otherwise specified)

Parameter	Condition	Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current [1]	T_c = 25℃	I_D	48	A
	T_c = 100℃		48	
Drain Current	T_a = 25℃	I_D	22	A
	T_a = 70℃		17.5	
Peak Drain Current, Pulsed [2]		I_{DM}	185	A
Power Dissipation [3]	T_c = 25℃	P_D	113.5	W
	T_c = 100℃		45.5	
Power Dissipation [4]	T_a = 25℃	P_{DSM}	6.2	W
	T_a = 70℃		4	
Single-Pulse Avalanche Current [2]		I_{AS}	28	A
Single-Pulse Avalanche Energy (L = 0.1 mH) [2]		E_{AS}	39	mJ
Operating and Storage Temperature Range		T_J, T_{stg}	- 55 to + 150	℃

Thermal Characteristics

Parameter	Condition	Symbol	Max.	Unit
Thermal Resistance-Junction to Ambient [4]	t ≤ 10 s	$R_{\theta JA}$	20	℃/W
Thermal Resistance-Junction to Ambient [4] [5]	Steady-State	$R_{\theta JA}$	50	℃/W
Thermal Resistance-Junction to Case	Steady-State	$R_{\theta JC}$	1.1	℃/W

[1] The maximum current rating is package limited.

[2] Single pulse width limited by junction temperature $T_{J(MAX)}$ = 150℃.

[3] The power dissipation P_D is based on $T_{J(MAX)}$ = 150℃, using junction to case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

[4] The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_a = 25℃. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t ≤ 10s value and the maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.

[5] The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

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Characteristics at T_a = 25℃ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at I_D = 250 μA	BV_{DSS}	100	-	-	V
Drain-Source Leakage Current at V_{DS} = 100 V	I_{DSS}	-	-	1	μA
Gate Leakage Current at V_{GS} = ± 20 V	I_{GSS}	-	-	± 100	nA
Gate-Source Threshold Voltage at V_{DS} = V_{GS}, I_D = 250 μA	$V_{GS(th)}$	1.3	-	2.3	V
Drain-Source On-State Resistance at V_{GS} = 10 V , I_D = 20 A at V_{GS} = 4.5 V , I_D = 20 A	$R_{DS(on)}$	- -	5.5 -	6.2 7.4	mΩ
DYNAMIC PARAMETERS					
Forward Transconductance at V_{DS} = 5 V, I_D = 20 A	g_{fs}	-	50	-	S
Input Capacitance at V_{GS} = 0 V, V_{DS} = 30 V, f = 1 MHz	C_{iss}	-	3860	-	pF
Output Capacitance at V_{GS} = 0 V, V_{DS} = 30 V, f = 1 MHz	C_{oss}	-	1520	-	pF
Reverse Transfer Capacitance at V_{GS} = 0 V, V_{DS} = 30 V, f = 1 MHz	C_{rss}	-	138	-	pF
Total Gate Charge at V_{GS} = 10 V, V_{DS} = 50 V, I_D = 20 A at V_{GS} = 4.5 V, V_{DS} = 50 V, I_D = 20 A	Q_g	- -	76 40	95 45	nC
Gate-Source Charge at V_{GS} = 10 V, V_{DS} = 50 V, I_D = 20 A	Q_{gs}	-	16	-	nC
Gate-Drain Charge at V_{GS} = 10 V, V_{DS} = 50 V, I_D = 20 A	Q_{gd}	-	20	-	nC
Turn-On Delay Time at V_{DS} = 50 V, V_{GS} = 10 V, R_L = 2.5 Ω, R_G = 3 Ω	$t_{d(on)}$	-	12	-	ns
Turn-On Rise Time at V_{DS} = 50 V, V_{GS} = 10 V, R_L = 2.5 Ω, R_G = 3 Ω	t_r	-	26	-	ns
Turn-Off Delay Time at V_{DS} = 50 V, V_{GS} = 10 V, R_L = 2.5 Ω, R_G = 3 Ω	$t_{d(off)}$	-	56	-	ns
Turn-Off Fall Time at V_{DS} = 50 V, V_{GS} = 10 V, R_L = 2.5 Ω, R_G = 3 Ω	t_f	-	35	-	ns
Body-Diode PARAMETERS					
Diode Forward Voltage at V_{GS} = 0 V, I_S = 1 A	V_{SD}	-	-	1	V
Body Diode Reverse Recovery Time at I_F = 20 A, di/dt = 200 A / μs	t_{rr}	-	50	-	ns
Body Diode Reverse Recovery Charge at I_F = 20 A, di/dt = 200 A / μs	Q_{rr}	-	156	-	nc

Electrical Characteristics Curves

Fig.1 Typical Output Characteristic

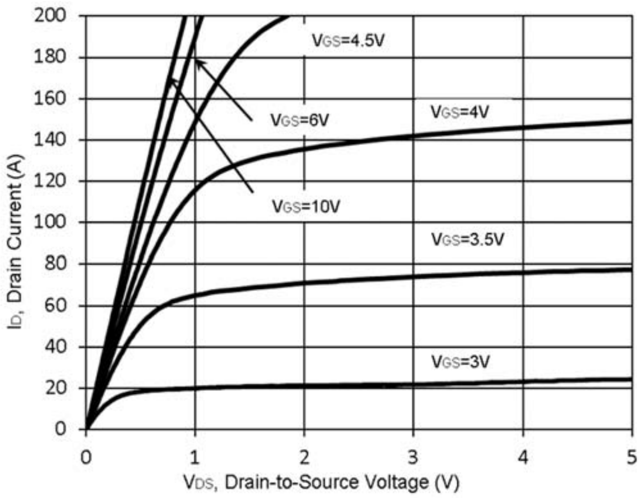


Fig.2 Typical Transfer Characteristic

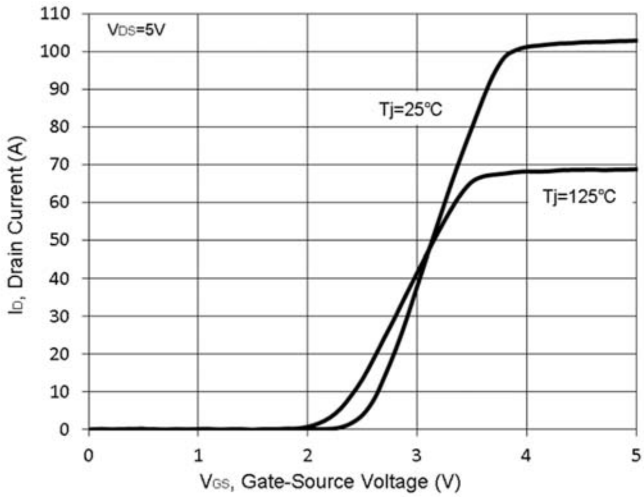


Fig.3 Diode Forward Voltage vs. Current

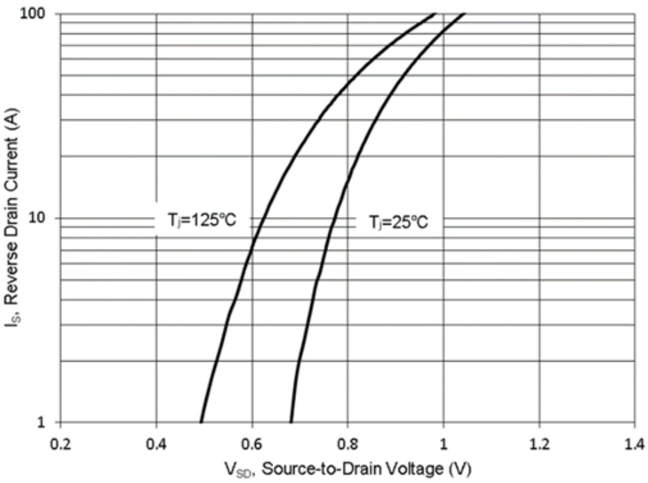


Fig.4 Typical on-Resistance vs. Drain Current

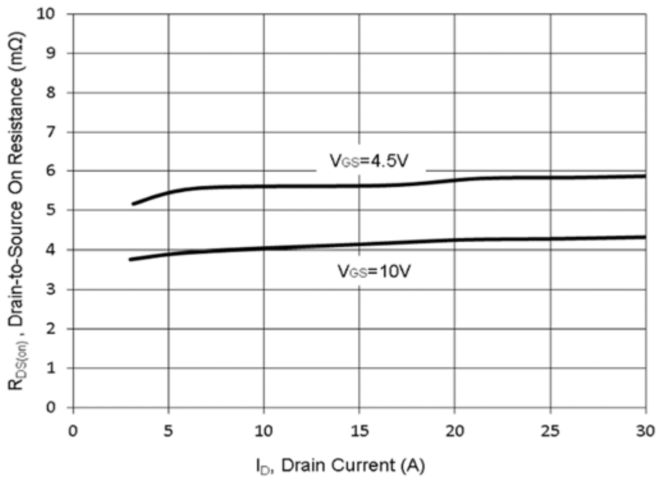


Fig.5 $V_{GS(th)}$ Variation vs. Temperature

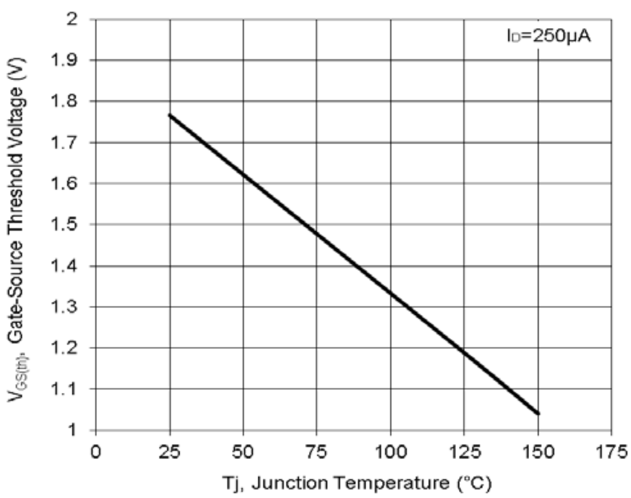
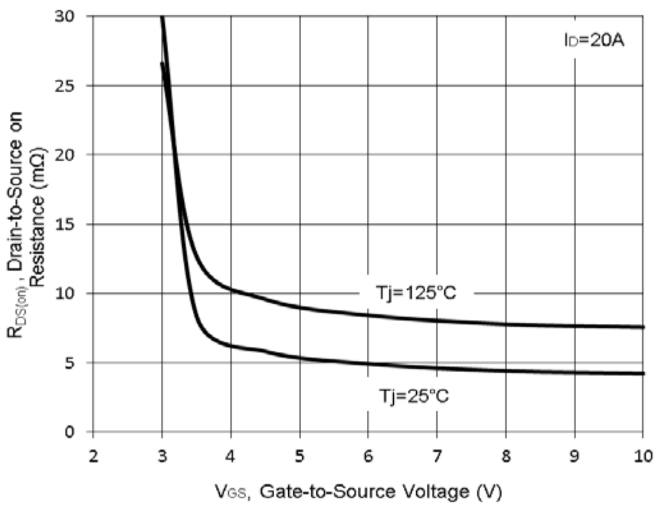


Fig.6 Typical on-Resistance vs. V_{GS}



Electrical Characteristics Curves

Fig.7 Gate Charge

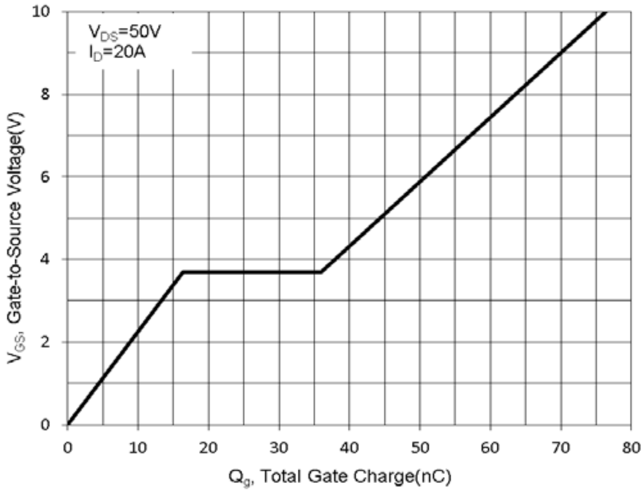


Fig.8 on-Resistance Variation vs. Junction Temperature

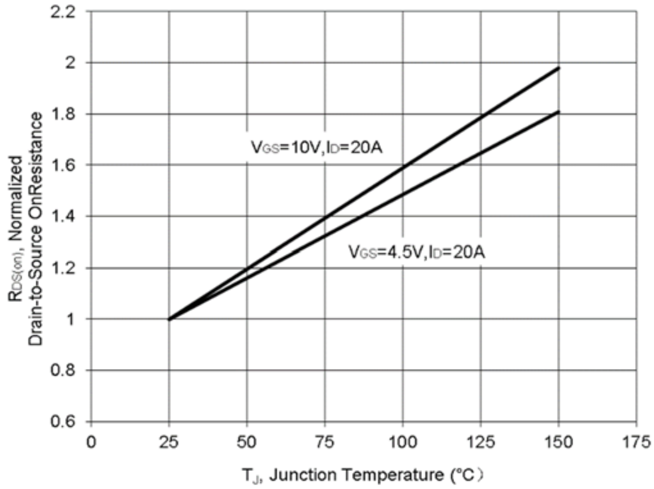


Fig.9 Typical Junction Capacitance

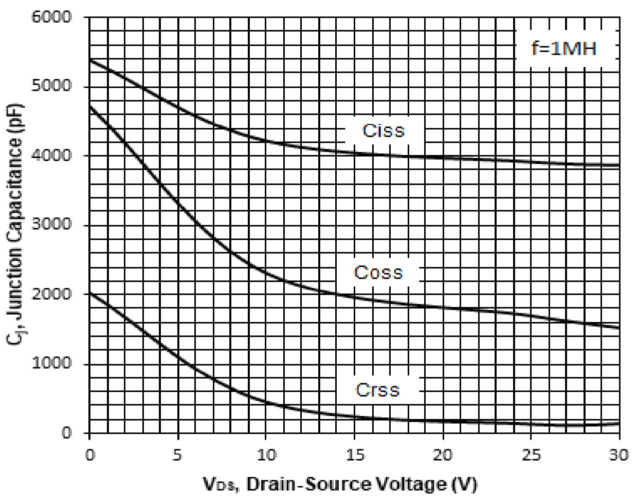
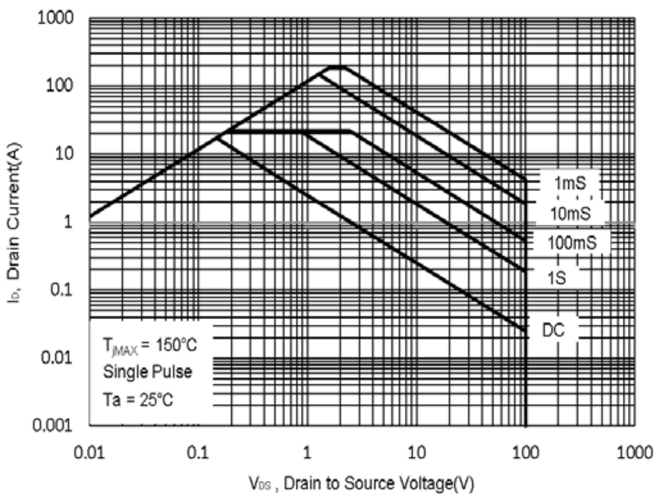


Fig. 10 Safe Operation Area



Test Circuits

Fig.1-1 Switching times test circuit

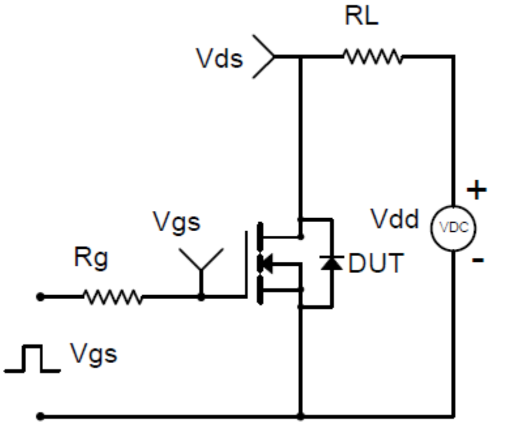


Fig.1-2 Switching Waveform

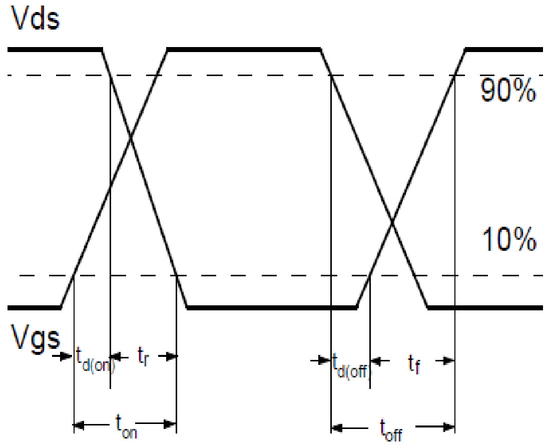


Fig.2-1 Gate charge test circuit

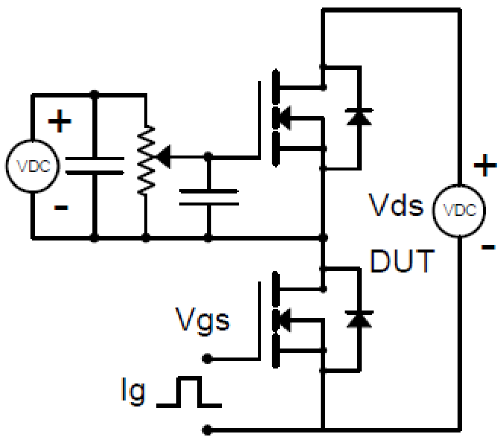


Fig.2-2 Gate charge waveform

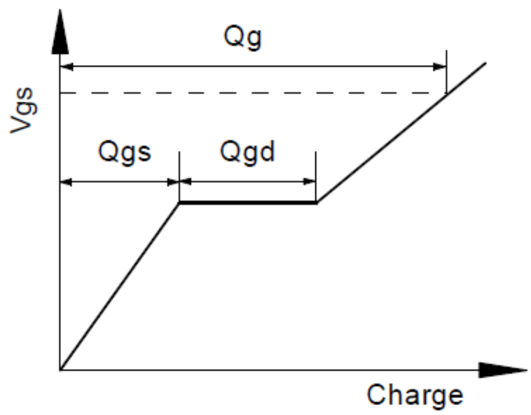


Fig.3-1 Avalanche test circuit

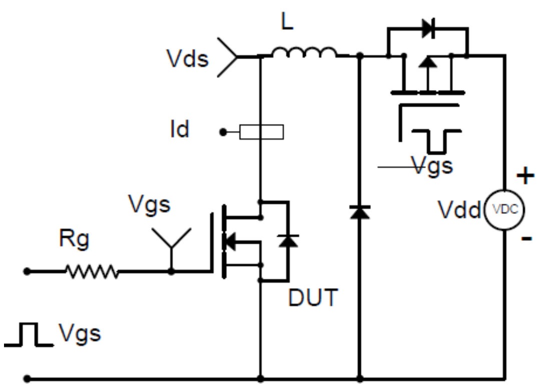
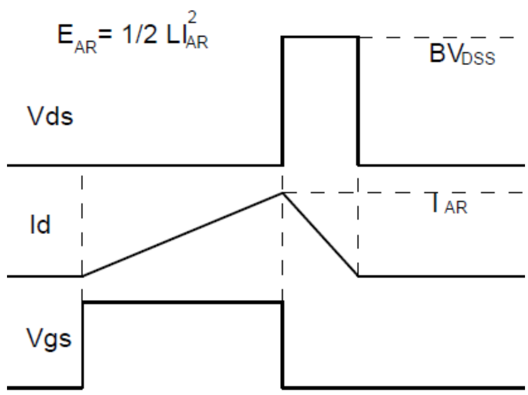
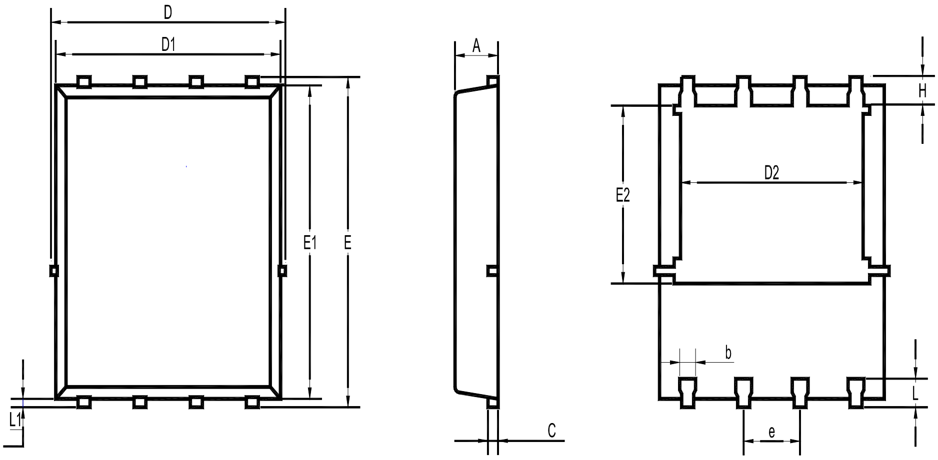


Fig.3-2 Avalanche waveform



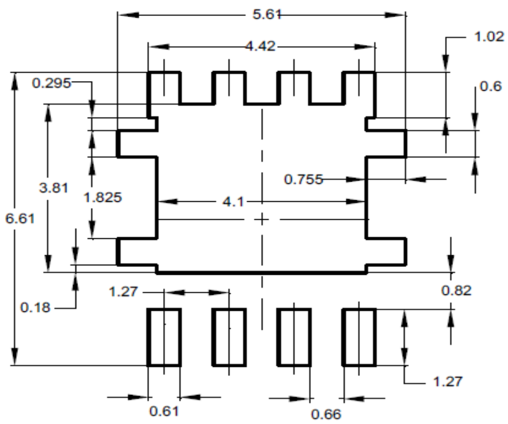
Package Outline Dimensions (Units: mm)

DFN5060



UNIT	A	b	C	D	D1	D2	E	E1	E2	e	L	L1	H
mm	1.12 0.9	0.51 0.33	0.34 0.11	5.26 4.7	5.1 4.7	4. 5 3.56	6.25 5.75	6 5.6	3.66 3.18	1.37 1.17	0.71 0.35	0.2 0.06	0.71 0.35

Recommended Soldering Footprint



Packing information

Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
DFN5060	12	8 ± 0.1	0.315 ± 0.004	330	13	3,000

Marking information

" TM510N062L " = Part No.

" ****** " = Date Code Marking

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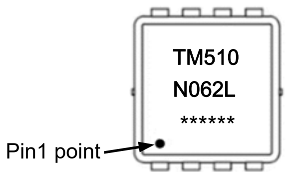

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